Integration of Ultra Low K Dielectric in a Semiconductor Fabrication Process

Abstract of the Disclosure

A backend semiconductor fabrication process includes forming an interlevel dielectric (ILD) overlying a wafer substrate by forming a low K dielectric (K<3.0) overlying the substrate of the wafer, forming an organic silicon-oxide glue layer overlying the low K dielectric, and forming a CMP stop layer dielectric overlying the glue layer dielectric. A void is then formed in the ILD, a conductive material is deposited to fill the void, and a polish process removes the excess conductive material. Forming the glue layer dielectric and the CMP stop layer dielectric is achieved by forming a CVD plasma using an organic precursor and an oxygen precursor and maintaining the plasma through the formation of the glue layer dielectric and the stop layer. The flow rate of the organic precursor is reduced relative to the oxygen precursor flow rate to form a CMP stop layer that is substantially free of carbon.